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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/863,978	05/23/2001	Ronald Clothier	END920000069US1	1420

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EXAMINER	
TRAN, BINH X	
ART UNIT	PAPER NUMBER
1765	6

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AS-6

Office Action Summary	Application No.	Applicant(s)	
	09/863,978	CLOTHIER ET AL.	
	Examiner	Art Unit	
	Binh X Tran	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *32-53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 54* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☒ Claim(s) *1-54* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-31, 54) in Paper No. 5 is acknowledged.

Claims 32-53 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 54 is indefinite because it depends on the non-elected claim 32.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3, 5-6, 12-14, 54 are rejected under 35 U.S.C. 102(e) as being anticipated by Asai et al. (US 6,240,636).

Asai discloses a structure comprising:

a carrier foil (10);

an electrically conductive layer (1) on one of the major surface of the carrier foil;

a dielectric layer (2) having circuitry feature (3);

a metal conductive circuitry located the circuitry features (i.e., inner wiring pattern 3) wherein the metal conductive circuitry is substantially flush/coplanar with and surrounded by the dielectric (2) (Fig 1, col. 2-3).

Respect to claim 3, Asai discloses the circuitry features in the dielectric layer (2) are formed short of the conductive layer (Fig 1). Respect to claim 5, Asai discloses the metal conductive circuitry (i.e., inner wiring pattern) comprises copper (col. 7 lines 17-20). Respect to claims 6, Asai discloses the dielectric layer (2) comprises an epoxy resin (col. 3 lines 16-20) or polyimide (col. 4 lines 41-42). "). Respect to claim 12, Asai discloses a cavity (i.e. via hole 5) exists through the dielectric layer (2) to the electricity conductive layer (1) wherein the cavity (via hole 5) resides an outer copper layer (6) (Fig 1, read on "the cavity resides an electronic component"). Respect to claim 13-14, Asai discloses the structure was attached together by a dielectric layer (4) (Fig 1, read on "stiffening dielectric

Respect to claim 54, Asai discloses a structure comprises: carrier foil (10), electrical conductive blanket (1), a dielectric material (2) with the circuitry features and a conductive metal to fill into the circuitry feature (Fig 1).

6. Claims 17, 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kataoka et al (US 6,270,889).

Kataoka discloses a structure comprising:

a base dielectric (6') (Fig 4);

a second dielectric layer (6) containing circuitry feature (8') (i.e. wiring pattern) located upon the base dielectric (6);

metal conductive circuitry feature (8') located within the circuitry feature wherein the metal conductive circuitry is substantially flush/coplanar with and surround by the second dielectric (6) (fig 4, col. 8-9).

Respect to claim 19, Kataoka teaches the metal conductive circuitry (wiring pattern) is made of copper (col. 8 lines 29-30). Respect to claims 20-21, Kataoka discloses the dielectric circuitry-containing layer and the dielectric base comprises epoxy resin or polyimide resin (col. 7 lines 60-65).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai in view of Tachibana (US 6,270,607).

Asai teaches a structure having a circuitry feature (3) in the dielectric layer (2). However, Asai fails to disclose the circuitry feature are formed completely through the

dielectric layer to the conductive layer. Tachibana teaches a structure having a circuitry features (3b) that are formed completely through the dielectric layer (3 or 1) to the conductive layer (2) (Fig 1). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asai in view of Tachibana by having the circuitry features run completely through the dielectric layer because it will allow to interconnect from both side.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai in view of Takayama et al. (US 5,977,783).

Respect to claim 8, Asai discloses the conductive layer comprises copper. Asai fails to disclose that conductive layer comprises chromium. Takayama teaches one can either use copper or chromium for conductive layer (col. 4 lines 51-59). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asai in view of Takayama by using chromium because equivalent and substitution of one for the other would produce an expected result.

10. Claims 4, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai in view of Hayashi (US 6,359,235).

Claim 4 differs from Asai by the specific value of circuitry width and spacing value. Hayashi discloses that the circuitry width and spacing values are result effective variables. Hayashi further discloses a circuit width of 20 μm (Note: 20 μm = 0.787 mil, read on applicants' range of 0.5-3 mil) and a spacing of 20μm (read on applicants' range of 0.5-1 mil, Col. 12 lines 11-20). The result effective variable is commonly determined by routine experiment. The process of conducting routine experiments so

as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it would have been obvious to one having ordinary skill in the art, at the time of invention, to perform routine experiment to obtain an optimal width and spacing as an expected result.

Respect to claims 9-10, Asai fails to disclose the flush metal conductive circuitry is covered with gold. However, Asai discloses a device with flush metal conductive circuitry. Hayashi discloses a flush metal circuitry (3) is covered or selectively covered with gold layer (4) (Fig 1E, col. 5 lines 35-45). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asai in view of Hayashi by covering a flush circuitry with a gold layer because this would decrease the resistance. Respect to claim 11, Hayashi discloses a gold wire bond (4) exist between gold covered circuitry layer (3) and layer (1) of the structure (Fig 1E, read on "between gold covered circuitry and other component").

11. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai in view of Miura et al. (US 5,768,108).

Respect to claims 15-16, Asai fails to disclose interconnecting from any layer of a conductive metal circuitry to any other layer of the conductive metal circuitry. However, Asia clearly discloses interconnect the conductive metal circuitry layer with the copper layer (6) (Fig 1). Miura discloses a device having a conductive metal circuitry (i.e. copper wiring) from one layer interconnect with a conductive metal circuitry from another layer (68) (col. 12 line 45 to col. 13 line 10, Fig 13). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asia in view of

Miura by interconnecting the conductive metal circuitry from one layer to another layer because this will help to create multi-layer wiring structure.

12. Claims 7, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai and Kataoka in view of each other.

Respect to claim 7, Asai fails to disclose the carrier foil comprises copper. Kataoka discloses the carrier foil is made of copper (col. 5 lines 1-5). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asai in view of Kataoka by using copper carrier foil because it is easy to bond with other layers.

Respect to claim 24, Kataoka fails to disclose a cavity exist through the dielectric layer to the metal conductive layer wherein the cavity having an electronic component. Asai discloses a cavity (i.e. via hole 5) exists through the dielectric layer (2) to the electricity conductive layer (1) wherein the cavity (via hole 5) resides an outer copper layer (6) (Fig 1, read on "said cavity resides an electronic component"). It would have been obvious to one having ordinary skill in the art, at the time of invention to modify Kataoka in view of Asai by having a cavity through the dielectric layer to the metal conductive layer because this would allow creating multi-layer interconnect. Respect to claims 25-26 Asai discloses the structure comprises repetitive layers and it is attached together by stiffening dielectric layer (4).

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka in view of Asai and Hayashi (US 6,359,235).

Kataoka fails to disclose the structure comprises repetitive layers and it is attached together by a dielectric layer. Asai discloses the structure comprises repetitive layers and it is attached together by a dielectric layer (4). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kataoka in view of Asai by attaching repetitive layers of said structure together by using a dielectric layer because this would allow creating multi-layer interconnect.

Claim 18 differs from Kataoka and Asai by the specific value of circuitry width and spacing value. Hayashi discloses that the circuitry width and spacing values are result effective variables. Hayashi further discloses a circuit width of 20 μm (Note: 20 μm = 0.787 mil, read on applicants' range of 0.5-3 mil) and a spacing of 20μm (read on applicants' range of 0.5-1 mil, Col. 12 lines 11-20). The result effective variable is commonly determined by routine experiment. The process of conducting routine experiments so as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it would have been obvious to one having ordinary skill in the art, at the time of invention, to perform routine experiment to obtain an optimal width and spacing as an expected result.

14. Claims 22-23, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka in view of Hayashi (US 6,359,235).

Respect to claim 22, Kataoka fails to disclose the flush metal conductive circuitry is covered with gold. However, Kataoka discloses a device with flush metal conductive circuitry. Hayashi discloses a flush metal circuitry (3) is covered or selectively covered with gold layer (4) (Fig 1E, col. 5 lines 35-45). It would have been obvious to one

having ordinary skill in the art, at the time of invention, to modify Kataoka in view of Hayashi by covering a flush circuitry with a gold layer because this would decrease the resistance. Respect to claim 23 Hayashi discloses a gold wire bond (4) exist between gold covered circuitry and layer (1) (Fig 1E, read on "attach exist ...other component").

Claims 29 differ from Kataoka by the specific value of circuitry width and spacing value. Hayashi discloses that the circuitry width and spacing values are result effective variables. Hayashi further discloses a circuit width of 20 μm (Note: 20 μm = 0.787 mil, read on applicants' range of 0.5-3 mil) and a spacing of 20μm (read on applicants' range of 0.5-1 mil, Col. 12 lines 11-20). The result effective variable is commonly determined by routine experiment. The process of conducting routine experiments so as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it would have been obvious to one having ordinary skill in the art, at the time of invention, to perform routine experiment to obtain an optimal width and spacing as an expected result.

15. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai and Kataoka in view of Miura.

Respect to claims 27-28, Asai and Kataoka fail to disclose interconnecting from any layer of a conductive metal circuitry to any other layer of the conductive metal circuitry. However, Asia clearly discloses interconnect the conductive metal circuitry layer with the copper layer (6) (Fig 1). Miura discloses a device having a conductive metal circuitry (i.e. copper wiring) interconnect with a conductive metal circuitry from another layer through layer (68) (col. 12 line 45 to col. 13 line 10, Fig 13). It would have

been obvious to one having ordinary skill in the art, at the time of invention, to modify Asia, Kataoka in view of Miura by interconnecting the conductive metal circuitry from one layer to another layer because this would allow creating multi-layer wiring film.

16. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka, Hayashi (US 6,359,235) further in view of Asai.

Respect to claim 30, Kataoka and Hayashi fail to disclose a cavity exist through the dielectric layer to the metal conductive layer wherein the cavity having an electronic component. Asai discloses a cavity (i.e. via hole 5) exists through the dielectric layer (2) to the electricity conductive layer (1) wherein the cavity (via hole 5) resides an outer copper layer (6) interconnect with the inner copper layer (Fig 1, read on "integrated circuit chip"). It would have been obvious to one having ordinary skill in the art, at the time of invention to modify Kataoka and Hayashi in view of Asai by having a cavity through the dielectric layer to the metal conductive layer because this would allow creating multi-layer interconnect.

Allowable Subject Matter

17. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X Tran whose telephone number is (703) 308-

1867. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin L Utech can be reached on (703) 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

Binh X. Tran
June 11, 2003

ROBERT KUNEMUND
PRIMARY EXAMINER